REMARKS

Claims 1-20 are now present in this application.

The specification and claims 1 and 4-10 have been amended, and claims 11-20 have been presented. Reconsideration of the application, as amended, is respectfully requested.

Rejection under 35 USC 112

Claims 4-6, 9 and 10 stand rejected under 35 USC 112, second paragraph. This rejection is respectfully traversed.

The Examiner has objected to the phrase "or its similar sequence". By way of the present amendment, applicant has cancelled the phrase "or its similar sequence."

Claims 1 and 7 stand rejected under 35 USC 112, second paragraph. This rejection is respectfully traversed.

The Examiner has indicated that "it is unclear how a difference signal between the reference wobble signal and the wobble pulse is generated". In view of the foregoing amendments, in which the claims have been amended to recite that "the difference signal is generated by comparing the phase of the reference wobble signal with the phase of the wobble pulse." It is also noted that newly presented claims 11-14 further discussed the methods and structure utilized to generate the difference.

In view of the foregoing amendments and remarks, it is respectfully submitted that all claims particularly point out and distinctly claim the subject matter of the instant invention. Accordingly, reconsideration and withdrawal of the rejections under 35 USC 112 are respectfully requested.

KM/asc

Rejection under 35 USC 102

Claims 1 and 7 stand rejected under USC 102(e) as being anticipated by Minamino et al., US Patent 6,657,929. This rejection is respectfully traversed.

The Examiner states that "*In regard to claim 1, An ADIP demodulation apparatus, which is applied to an optical disk driver to generate ADIP information according to a wobble signal, the ADIP demodulation apparatus comprising (column 6 lines 42-47) : a slicing unit for receiving the wobble signal and generating a wobble pulse by slicing the wobble signal (fig. 9 element 13); a phase locked loop for generating a reference wobble signal with the same frequency and phase as the wobble pulse according to the wobble pulse (fig. 9 element 14 see also column 12 lines 42-53); a channel bit generator for generating a channel bit signal according to the reference wobble signal and the wobble pulse (fig. 9 element 8); and a decoder for decoding to the ADIP information according to the channel bit signal (fig. 9 element 7); wherein the channel bit generator generates a difference signal between the reference wobble signal and the wobble pulse and generates the channel bit signal according to the difference signal (fig. 9 element 15b).*"

The purpose of the Minamino et al. patent is to generate a correct wobble PLL clock (wobble signal) being synchronous with the wobbling on the disk, by using the wobble signal processing block 70 as shown in Fig. 9. However, the purpose of the present application is to generate an ADIP (Address In Pre-Groove) information according to a wobble signal. In other words, Minamino et al. teaches how to generate a wobble signal, not how to generate a signal dependent upon a wobble signal. More specifically, Minamino et al. does not teach how to

generate ADIP information. Accordingly, the purpose and structure of the present invention differ from those of Minamino et al.

Element 8 in Fig. 9 of Minamino et al. is a formatter, which not only receives the output signal of the wobble PLL circuit 14 but also receives the output signals of wobble PLL detection circuit 15b, the reproduced signal processing circuit 6 and RISC processing section 9. The formatter 8 generates a plurality of signals for outputting to the recording pulse generation circuit 7, the wobble digitizing circuit 13, the wobble PLL detection circuit 15b, the reproduced signal processing circuit 6 and the RISC processing section 9. As described in column 8, lines 4-7 of Minamino et al., the formatter 8 performs demodulation and error checking for signals corresponding to the plurality of physical IDs located at the head of a sector in the digital data reproduced by the reproduced signal processing circuit 6. However, the channel bit generator in the present application receives the output signal of slicing unit 21, the output signal of PLL 23 and the reference clock WCK of the clock generator 22 and generates the channel bit signal. The channel bit generator in the present invention does **not** perform the functions of demodulation and error checking. Therefore, the function and structure of the channel bit generator in the present application differ from the formatter of Minamino et al.

Moreover, in Fig. 9 of Minamino et al. , the wobble signal processing block 70 is used to generate wobble signal, and comprises the polarity selection circuit 11, the bandpass filter 12, the wobble digitizing circuit 13, the wobble PLL circuit 14, the wobble signal lock detection circuit 17 and the wobble PLL detection circuit 15b. The recording pulse generation circuit 7 and the formatter 8 are not included in the wobble signal processing block 70. The wobble signal processing block 70 is used to generate a wobble signal, and is not used to generate ADIP

information. The recording pulse generation circuit 7 is used to generate a recording pulse to the laser driving circuit. However, the decoder in the present application is used to decode the ADIP information according to the channel bit signal. Therefore, the function and structure of the decoder of the present application differ from those of the recording pulse generation circuit 7 in Minamino et al.

Therefore, Minamino et al. neither teaches nor suggests how to generate a channel bit signal by a difference signal generated by executing XOR function between the reference wobble signal and the wobble pulse, and generate ADIP (Address in Pre-Groove) information.

Accordingly, it is respectfully submitted that the prior art utilized by the Examiner fails to teach or suggest the apparatus and method of independent claims 1 and 7, as well as their dependent claims. Reconsideration and withdrawal of the 35 USC 102 rejection are respectfully requested.

Rejection under 35 USC 103

Claims 8-10 stand rejected under USC 103 as being obvious over Minamino et al. in view of the Applicant's Admitted Prior Art. This rejection is respectfully traversed.

The Examiner states that "*In regard to claims 8-10, Minamino et al. teaches the elements of claims 8-10 except the ADIP information is a sync data when the channel bit signal sequence is 11110000 or its similar sequence; the ADIP information is data 0 when the channel bit signal sequence is 10000011 or its similar sequence; and the ADIP information is a sync data when the channel bit signal sequence is 10001100 or its similar sequence*".

As discussed above, the purpose of Minamino et al. is to generate a correct wobble PLL clock (wobble signal) being synchronous with the wobbling on the disk by using the wobble signal processing block 70, as seen in Fig. 9. However, the purpose of the present application is to generate ADIP (Address In Pre-Groove) information according to a wobble signal. Since claims 8-10 depend directly or indirectly on claim 7, these claims should be considered allowable for the same reasons recited above, as well as for the additional limitations recited therein.

Accordingly, it is respectfully submitted that the prior art utilized by the Examiner fails to teach or suggest the method of independent claim 7, as well as its dependent claims 8-10. Reconsideration and withdrawal of the 35 USC 103 rejection are respectfully requested.

Conclusion

Favorable reconsideration and an early Notice of Allowance are earnestly solicited.

Because the additional prior art cited by the Examiner has been included merely to show the state of the prior art and has not been utilized to reject the claims, no further comments concerning these documents are considered necessary at this time.

In the event that any outstanding matters remain in this application, the Examiner is invited to contact the undersigned at (703) 205-8000 in the Washington, D.C. area.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

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